IN THE CLAIMS:

Please amend the claims as indicated below. Claims 31-38 have been added. Below are the amended claims in clean, unmarked format.

1. (Amended) An apparatus comprising:

a clock distribution network to distribute a clock signal on an integrated circuit chip; and

a duty cycle correction circuit at a receiver in the clock distribution network, the duty cycle correction circuit to correct a duty cycle of a distributed clock signal received at the receiver.

6. (Amended) A clock distribution network comprising:

clock generation circuitry at a first location to generate a global clock signal;

clock distribution circuitry to distribute the global clock signal on an integrated circuit chip from the clock generation circuitry to a receiving point at a second, different location on the integrated circuit chip; and

a duty cycle correction circuit at the receiving point to correct the duty cycle of the distributed global clock signal received via the clock distribution circuitry.

10. (Amended) The clock distribution network of claim 9 wherein a signal communicated via the feedback path in the duty cycle correction circuit is to control at least one variable delay element in the duty cycle correction circuit.

11. (Amended) The clock distribution network of claim 6 wherein the duty cycle correction circuit provides a corrected output clock signal having a substantially 50% duty cycle.

18. (Amended) An integrated circuit chip comprising:

a clock generation circuit to provide a first clock signal having a first duty cycle;

a clock distribution network coupled to the clock generation circuit to distribute the first clock signal across the integrated circuit chip; and

a plurality of duty cycle correction circuits at receiving points in the clock distribution network, the duty cycle correction circuits to correct a duty cycle of the first clock signal at the receiving points.

19. (Amended) The integrated circuit chip of claim 18 wherein at least one of the duty cycle correction circuits is coupled to frequency multiplying circuitry.

20. (Amended) The integrated circuit chip of claim 19 wherein the duty cycle correction circuits are to correct the duty cycle of the first clock signal to be substantially a 50% duty cycle.

21. (Amended) The integrated circuit chip of claim 18 wherein at least one of the duty cycle correction circuits is coupled to smart buffer circuitry to provide for proper operation of the at least one duty cycle correction circuit for a range of loads to be coupled to an output of the at least one duty cycle correction circuit.

28. (Amended) A method comprising:

receiving an input clock signal from a clock distribution network on an integrated circuit chip at an endpoint of the clock distribution network; and

correcting the duty cycle of the input clock signal at the endpoint to provide a corrected output clock signal.

31. (New) The apparatus of claim 2 further including:

a sense amplifier in the feedback path, the sense amplifier having a threshold substantially equal to one half of the supply voltage (Vcc) to be coupled to the circuit.

32. (New) The apparatus of claim 31 further including:

a reset path between an input of the duty cycle correction circuit and an output of the duty cycle correction circuit, the reset path to control a width of the output clock signal.

33. (New) The apparatus of claim 33 wherein each of the reset path and the feedback path is coupled to control a variable delay element.

34. (New) The apparatus of claim 5 wherein the smart buffer circuit is to match a delay of an output signal from the duty cycle correction circuit to a delay of a reference signal independent of a load coupled to the duty cycle correction circuit over the range of loads, the smart buffer circuit to adjust the delay of the output signal by adjusting the drive strength of an output driver in the duty cycle correction circuit.

35. (New) The apparatus of claim 34 wherein the smart buffer includes

a first phase detector to detect a difference in delay between one of a rising or falling edge of the output signal and a corresponding edge of the reference signal, the first phase detector to provide a first reference control signal at an output, the first reference control signal to control a delay of a first delay element in the duty cycle correction circuit to adjust the drive strength of the driver for a first value of an input signal to the duty cycle correction circuit.

36. (New) The apparatus of claim 35 wherein the smart buffer circuit further includes

a second phase detector to detect a difference in delay between a remaining one of a rising or falling edge of the output signal and a corresponding edge of the reference signal, the second phase detector to provide a second reference control signal at an output, the second reference control signal to control a delay of a second delay element in the duty cycle correction circuit to adjust the drive strength of the output driver for a second value of the input signal to the duty cycle correction circuit.

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37. (New) The apparatus of claim 1 wherein the duty cycle correction circuit is to receive the distributed clock signal and to generate a reference voltage signal, a voltage of the reference voltage signal to vary in response to a change in frequency of the input clock signal, the apparatus further comprising,

a clock generation circuit to receive the reference voltage signal and to provide an output clock signal, the clock generation circuit to vary the delay of the output clock signal in response to a variation in voltage of the reference voltage signal.

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38. (New) The apparatus of claim 37 wherein the clock generation circuit is to provide multiple output clock signals, each of the multiple output clock signals to vary in response to a variation in the voltage of the reference voltage signal.